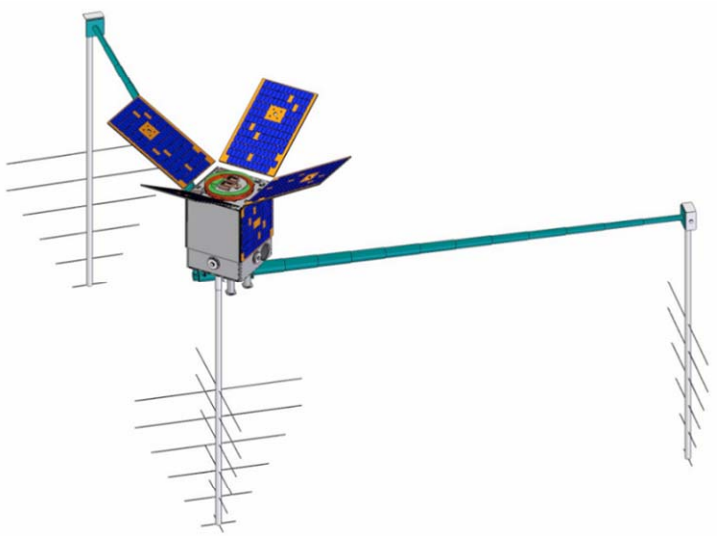
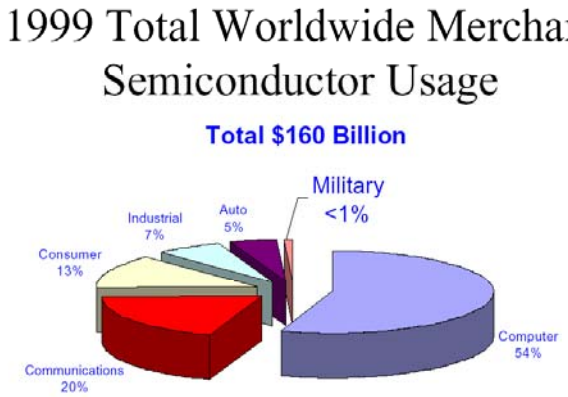
Results from the Cibola Flight Experiment's 1st Year



Michael Caffrey
Keith Morgan
Anthony Salazar
Diane Roussel-Dupre

Rad-Hard Space Processing: Lags ground-based processing by 10 years!

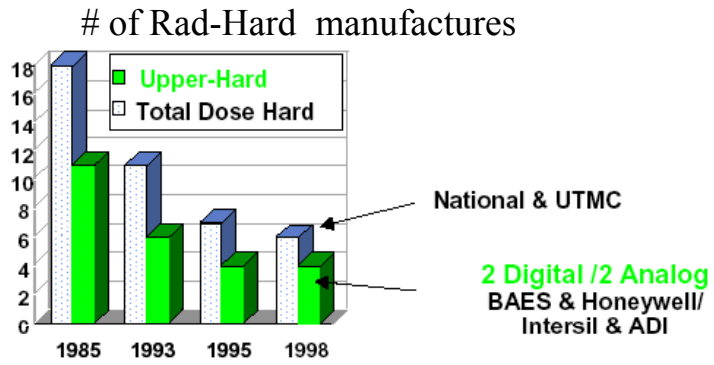


Exponential increase in cost to fabricate

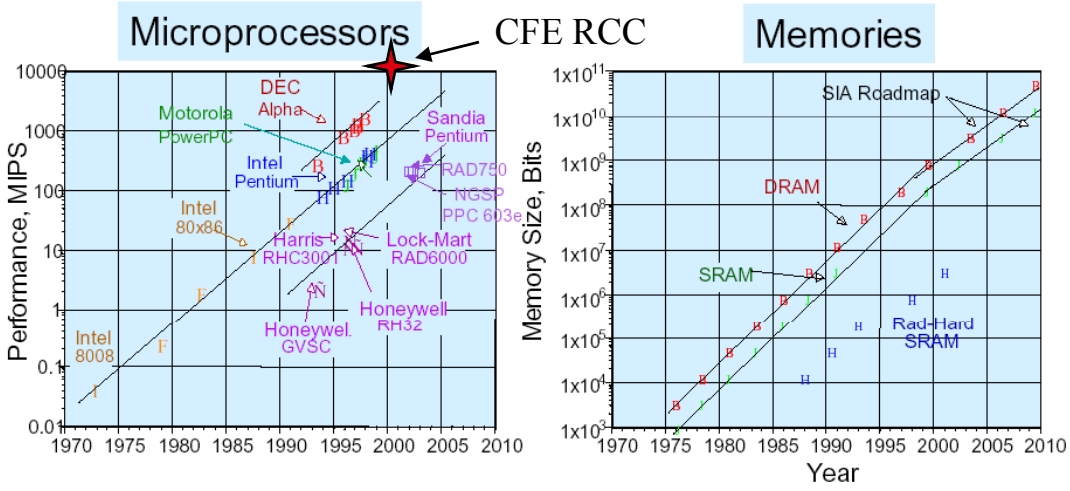
Source: SIA, IC Insights

Average cost of .35µ 200mm Fab= $880/M

Average cost of .25µ 200mm Fab=$1329/M



*DTRA 1999



Rad-Hard Lags 2-3 Generations Behind Commercial

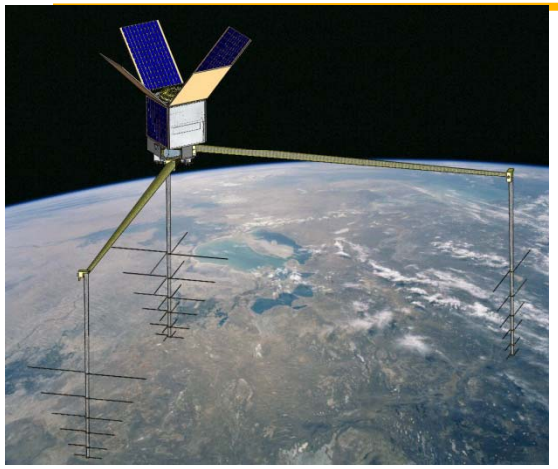
- Milspace small % of market
- Disappearing Rad-Hard foundries
- Eroding Rad-Hard Market
  commercial space weak
- Low Volume Demand

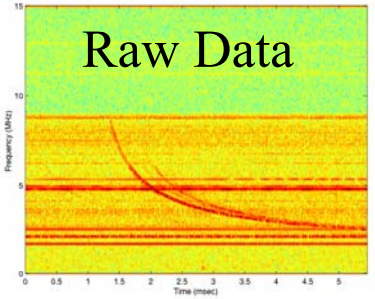
->Difficult times ahead for space processing

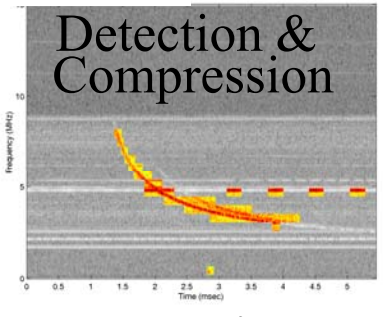
->Need alternate technologies to meet needs

CFE Concept

"Continuous, full bandwidth signal processing to deliver real-time data products to users"







Technology Demonstration:

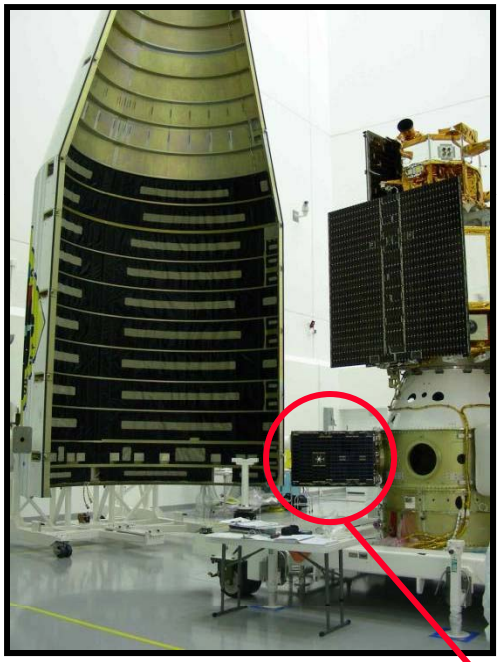
- **FPGA based parallel computing offers 100x performance advantage and adaptability**
  - Processing gain => greater sensitivity, data reduction
  - Reprogrammable => combats mission obsolescence, leverages new algorithms/targets after launch
- **Leveraging COTS technology**
  - Reuse of commercial design tools, foundry, processes, masks
    - Reduces lead time vs ASICs
    - Reduces validation and verification time
    - Enhances Government access to commercial process geometries
    - Reduced cost (per part and foundry chasing costs)
  - Fabricated on epi substrate for SEL immunity
  - Challenges
    - Single Event Upset must be handled at system level
    - Relatively high power density and complex packaging issues
    - Parallel computing not necessarily right hammer for all problems

Description:

- **Orbit: Circular 560 Km, 35.4 degree inclination**
- **Software Radio:**
  - Four channels, 20 MHz bandwidth each
  - Tunable from 100 to 500 MHz,
  - 300 Gop/sec Re-Configurable Computer (RCC)
  - 4-element antenna array

CFE Project Highlights

Space Launch by STP (STP-1)

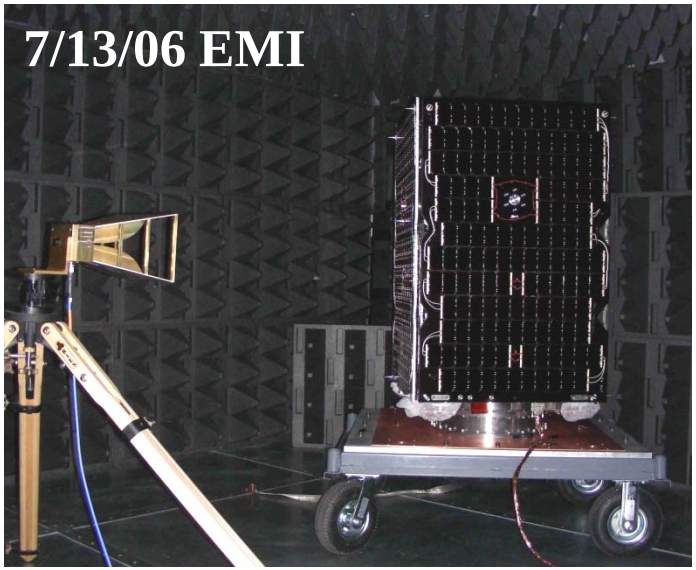


CFE mated to launch adapter

Los Alamos NATIONAL LABORATORY EST.1943

NNSA

FY06 CFE Project Highlights



6/15/06 Integrate Payload

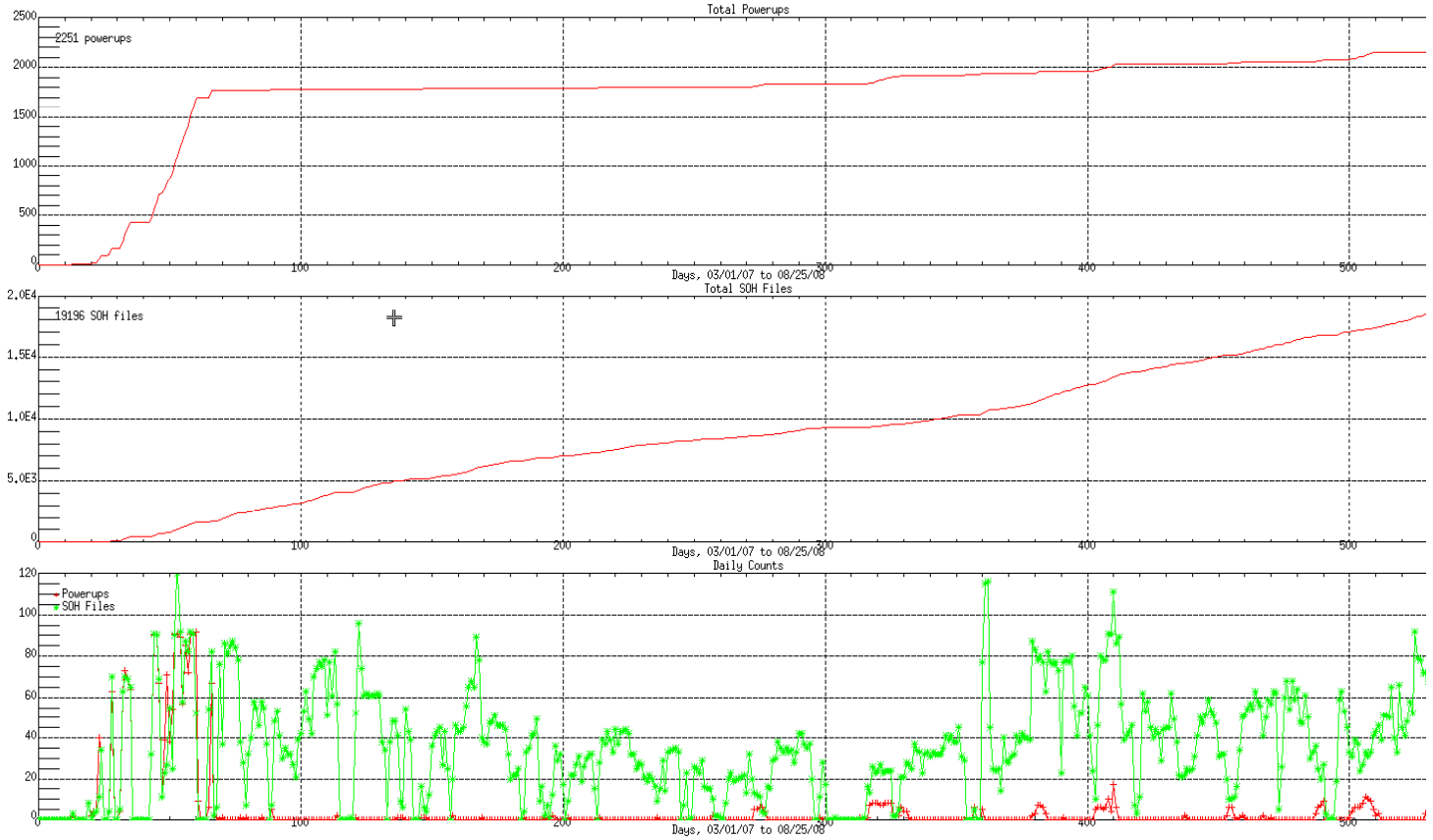
Statistics Summary

>18,000 Experimen
>32 UPLOADS

From 03/01/07 to 08/25/08

18565 SOH files
17 GB SOH, 244 GB SCI

Payld	9678.2 hrs	74.26%
Radio	2010.8 hrs	15.43%
R1-FA	3857.7 hrs	29.60%
R1-FB	3742.3 hrs	28.72%
R1-FC	3744.2 hrs	28.73%
R2-FA	3856.4 hrs	29.59%
R2-FB	3738.6 hrs	28.69%
R2-FC	3738.9 hrs	28.69%
R3-FA	3774.0 hrs	28.96%
R3-FB	3772.9 hrs	28.95%
R3-FC	3769.1 hrs	28.92%

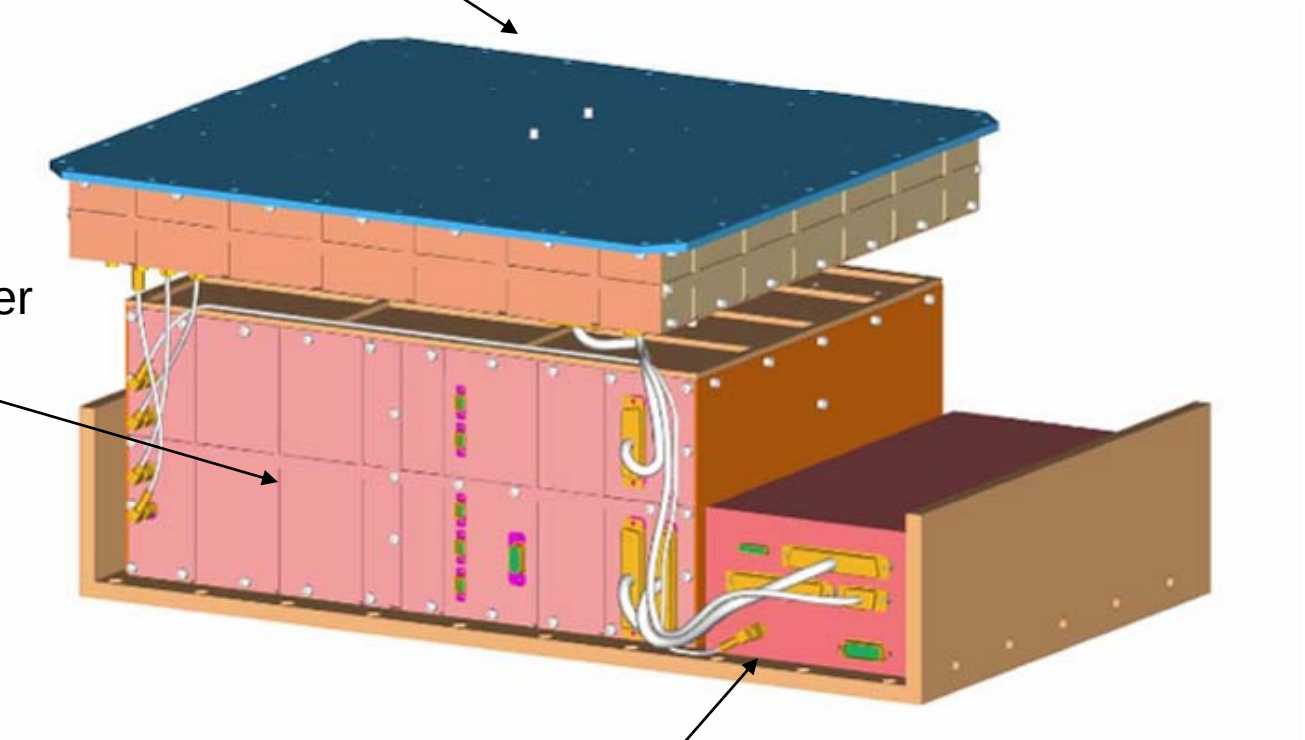


*seeduty,'2007-03-01','2008-04-15'
*onoff,startTime,endTime,pSym=pSym,DEBUG=DEBUG,PRINTTIMES=PRINTTIMES,maxTimes=maxTimes

CFE Payload

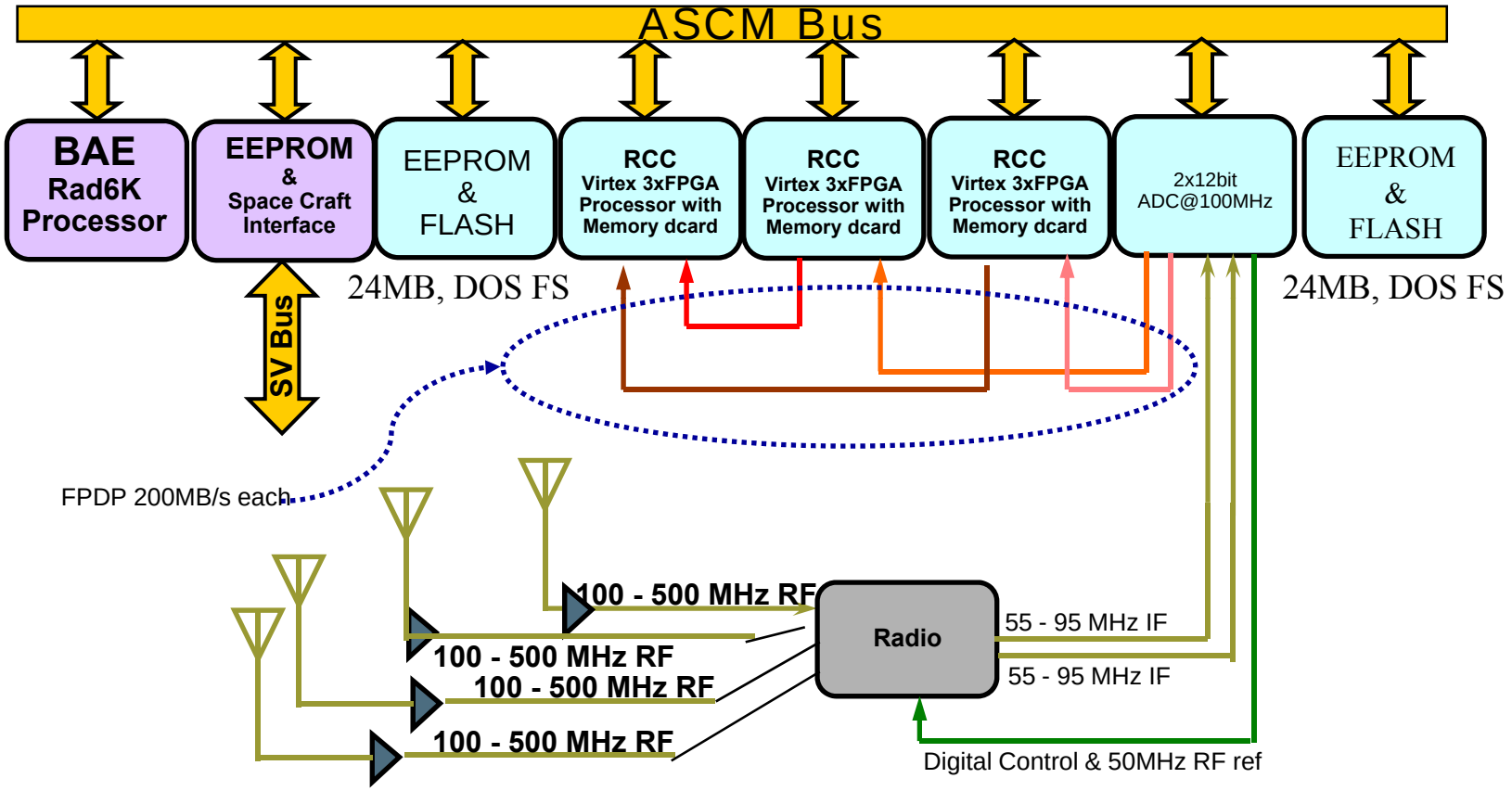
4x 20MHz Radios, 100-500MHz

Reconfigurable computer



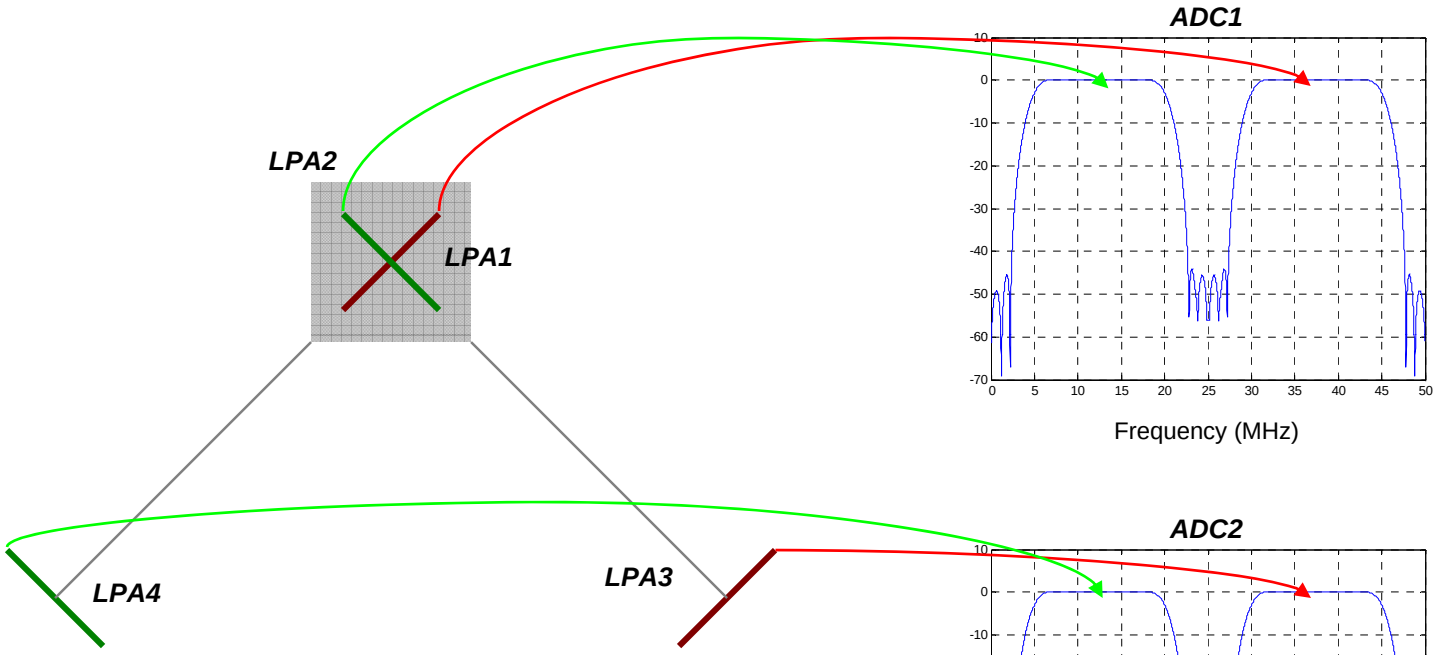
Powersupply

Payload Block Diagram



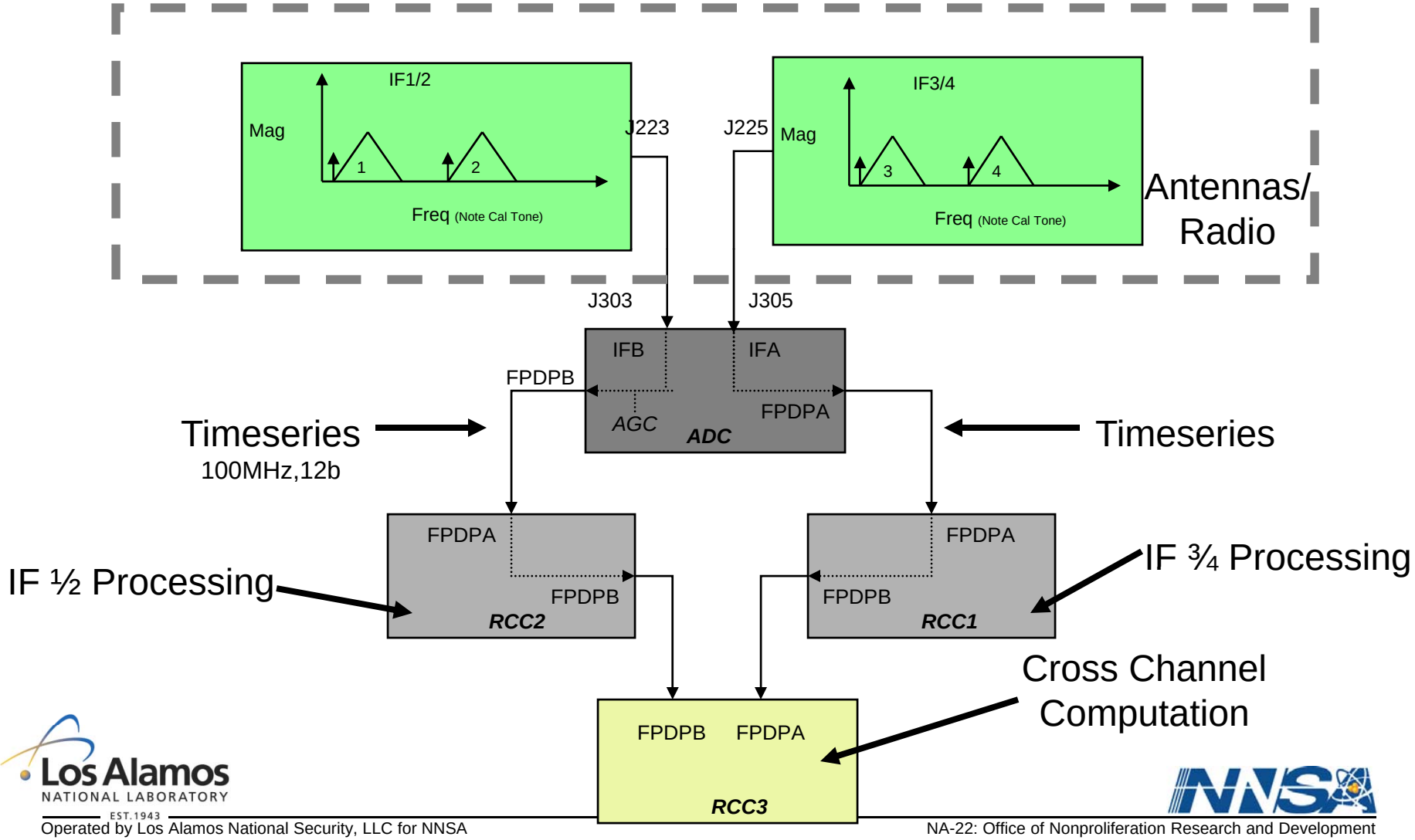
four 20MHz wide radio channels, gang tuned
2 channels combined into each 50MHz RCC input

RF Signal Flow

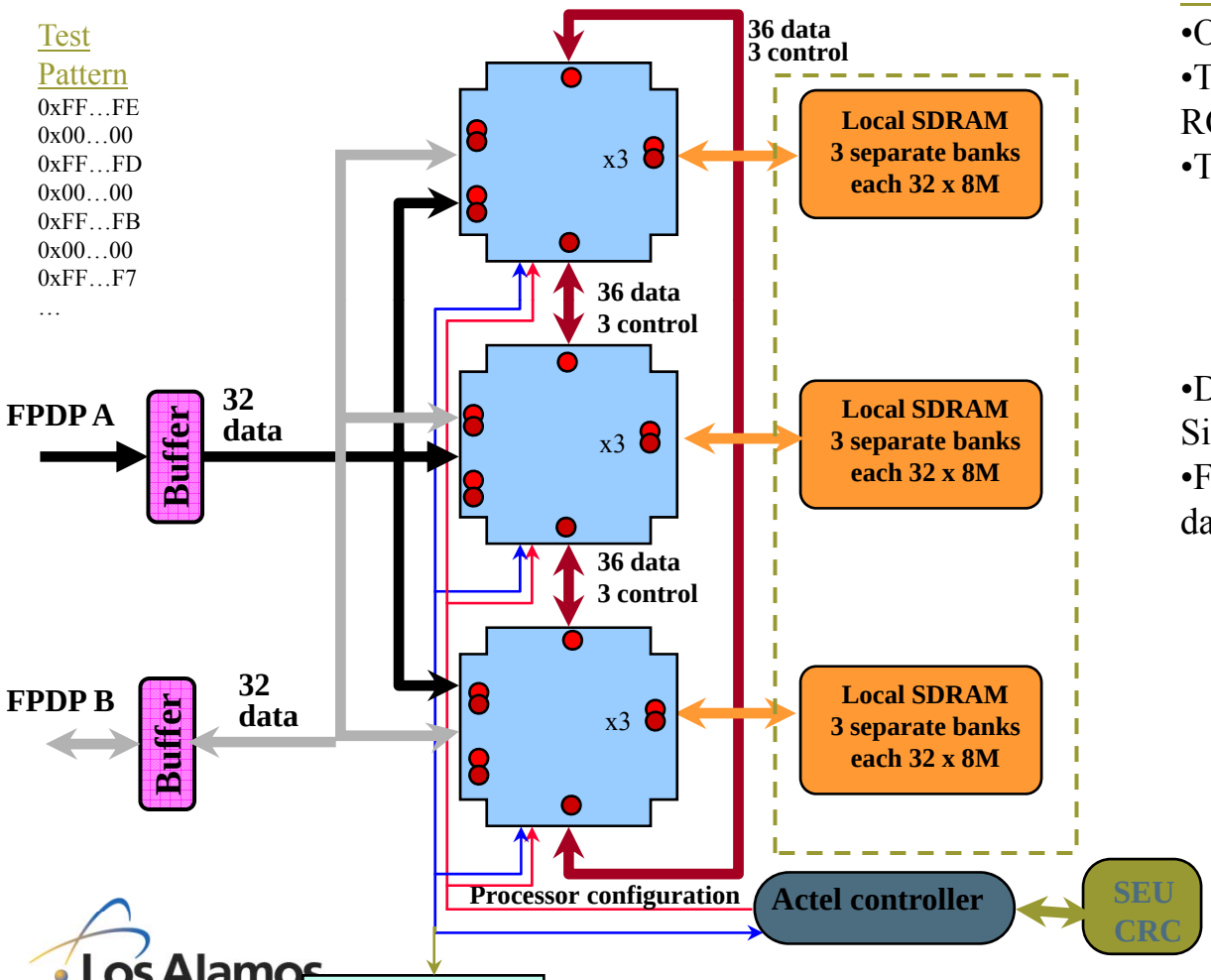


- **Two baseline interferometer**
- **Antenna pairs occupy same portion of the spectrum**
- **Bandpass sampled (spectrum inverted)**
- **RF 100 – 500 MHz**
- **Instantaneous Bandwidth ~18 MHz**

Data Flow


IF1/2
Mag
1
2
Freq (Note Cal Tone)
J223
J225
IF3/4
Mag
3
4
Freq (Note Cal Tone)
Antennas/
Radio
J303
J305
IFB
IFA
FPDPB
AGC
FPDPA
ADC
Timeseries
100MHz,12b
Timeseries
FPDPA
FPDPB
RCC2
IF ½ Processing
FPDPA
FPDPB
RCC1
IF ¾ Processing
Cross Channel
Computation
FPDPB
FPDPA
RCC3

RCC Module Architecture & Testability



Built in test will Fly

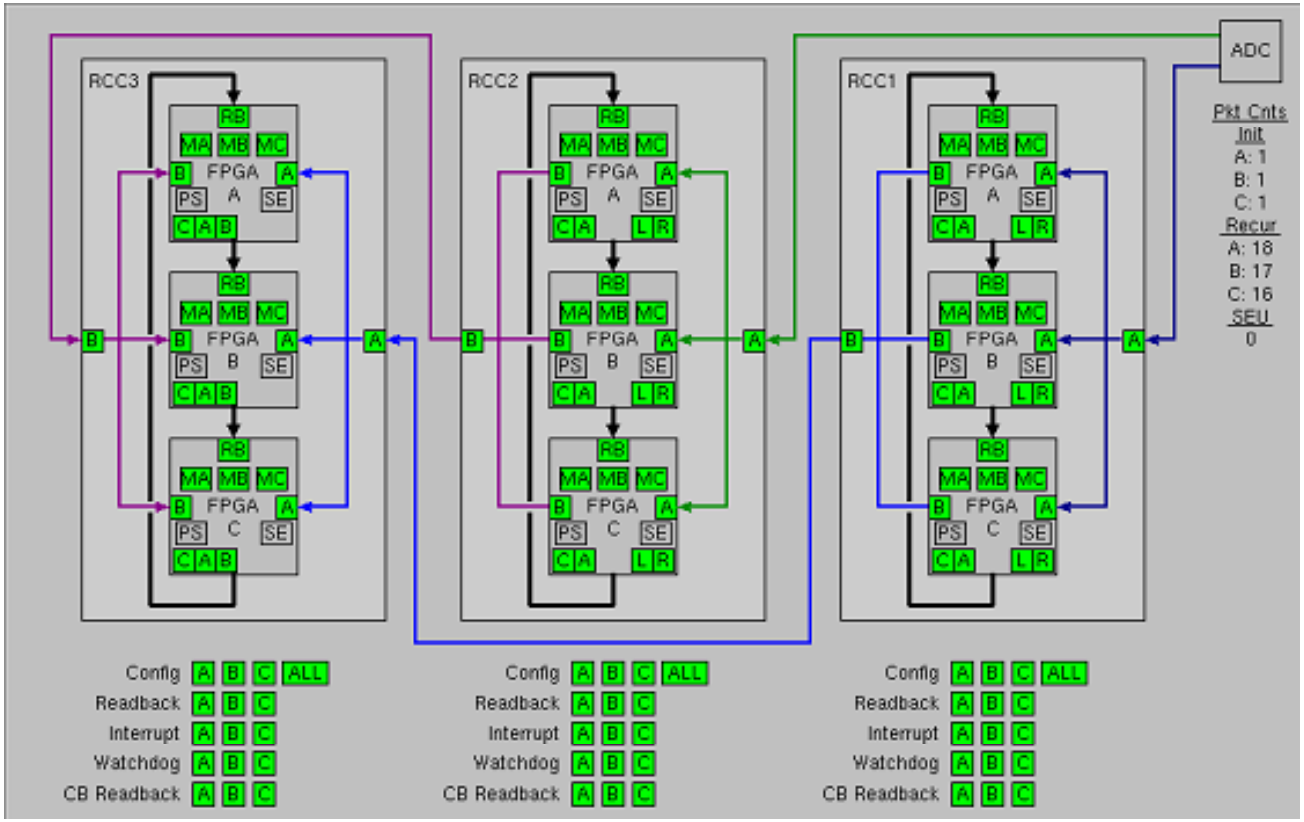
- One test configuration for 9 XQVR1000
- Tests system from ADC module through 3 RCC modules
- Tests for
  - Opens
  - Shorts
  - Ground Bounce
  - Crosstalk
- Does NOT test Si, working with Xilinx on Si test ideas for XQVR1K
- Fault isolation via verifier ID and failure data pattern

SEU Insertion

- Microprocessor can inject 'SEUs' into the bitstream of the XQVR1K for observing upset consequences and testing system response

- Verify Test Pattern
- Generate Test Pattern

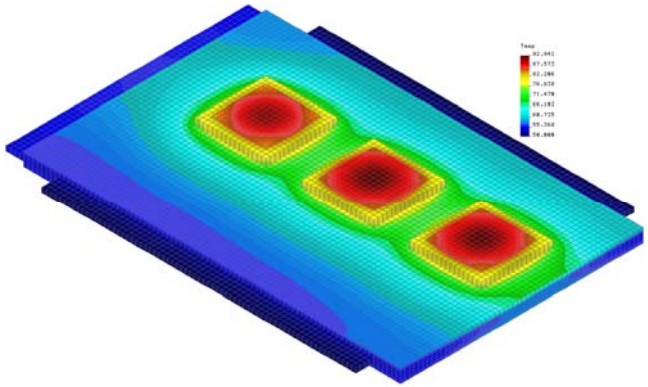
Payload Built in Self Test



- Tests Data path from ADC
- Memory Interface
- Processor Interface
- Interrupt
- SEU Detection
- X triggers
- Power Load

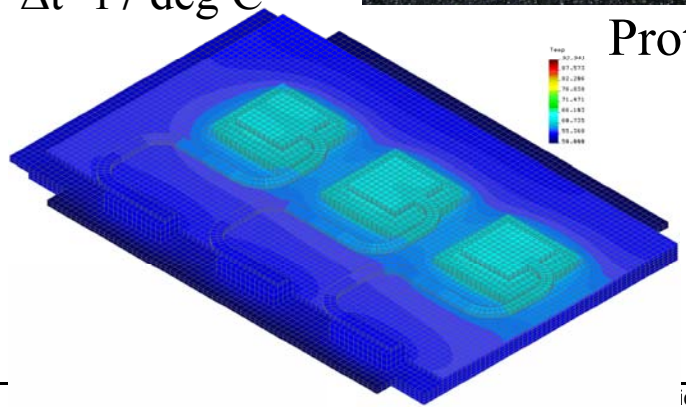
Power = f(algorithm)

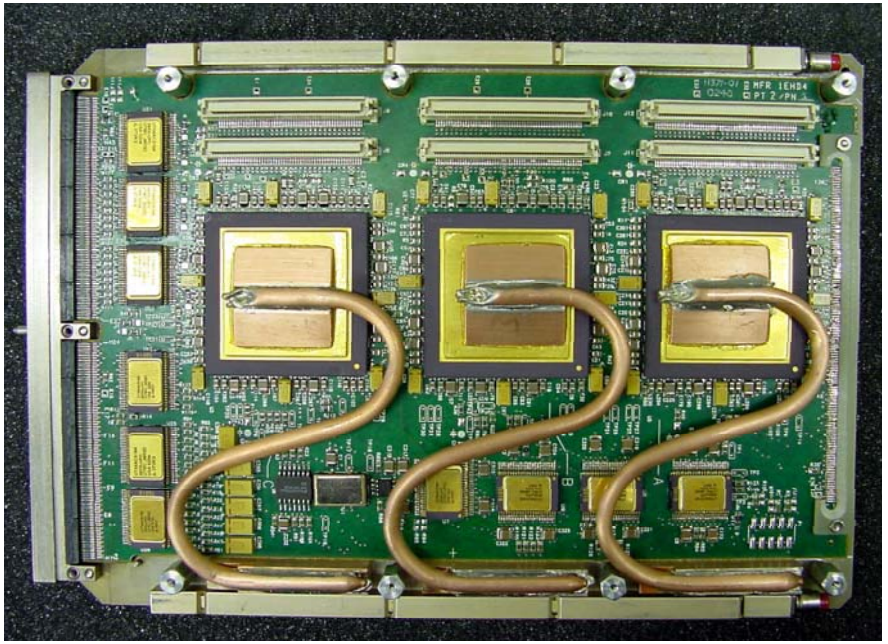
- **Each RCC board power usage ≈5 - 28W**
- **Each FPGA has >500 pins which are susceptible to thermal stresses**
  - Maximize lifetime
    - Heat pipes limit max temperatures
    - Column Grid Array package more reliable
    - Matched CTE of thermount PCB to Ceramic Pkg
    - AlBeMet core has superior thermal transfer



Without heat pipes:
Δt=50 deg C

With heat pipes:
Δt=17 deg C





ProtoFlight RCC Board

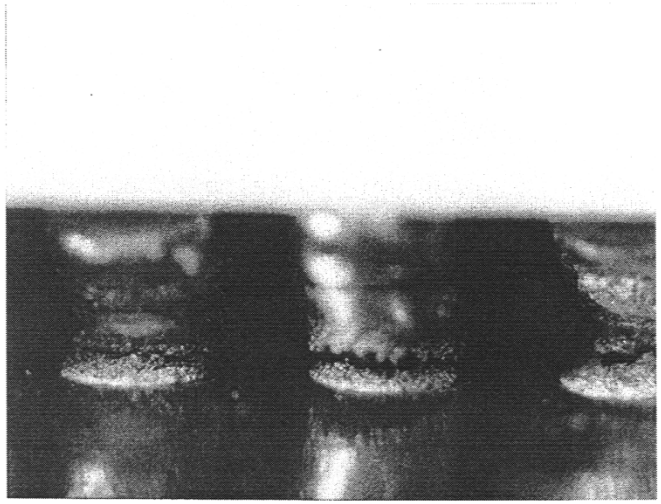
Package Reliability

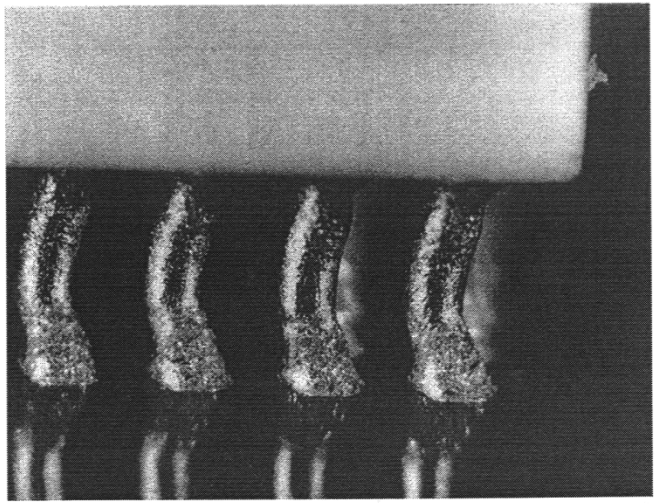
STC Semiconductor Technology Center, Manassas, VA

STC Packaging Development

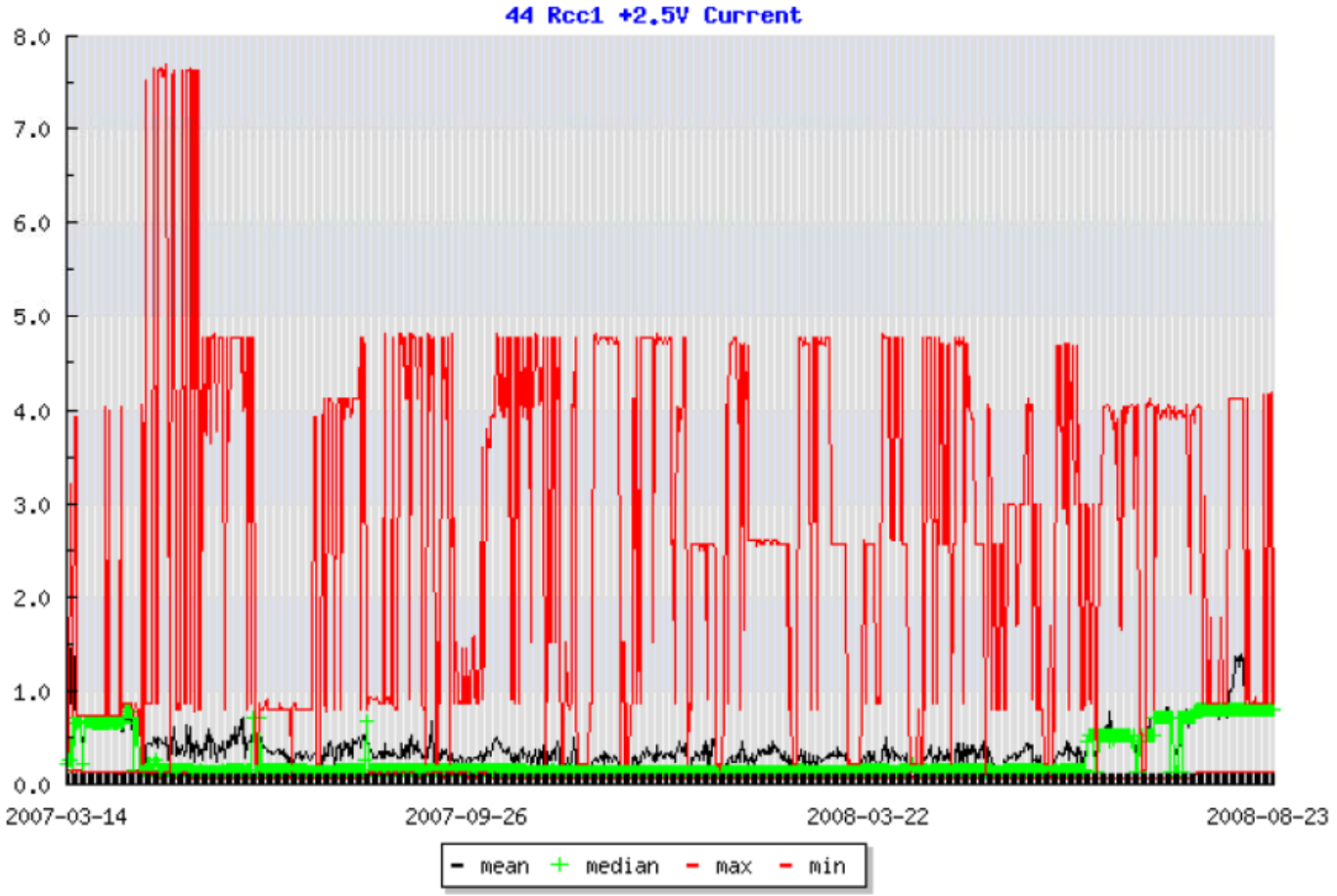
LOCKHEED MARTIN

CGA Flexture vs. BGA Fracture

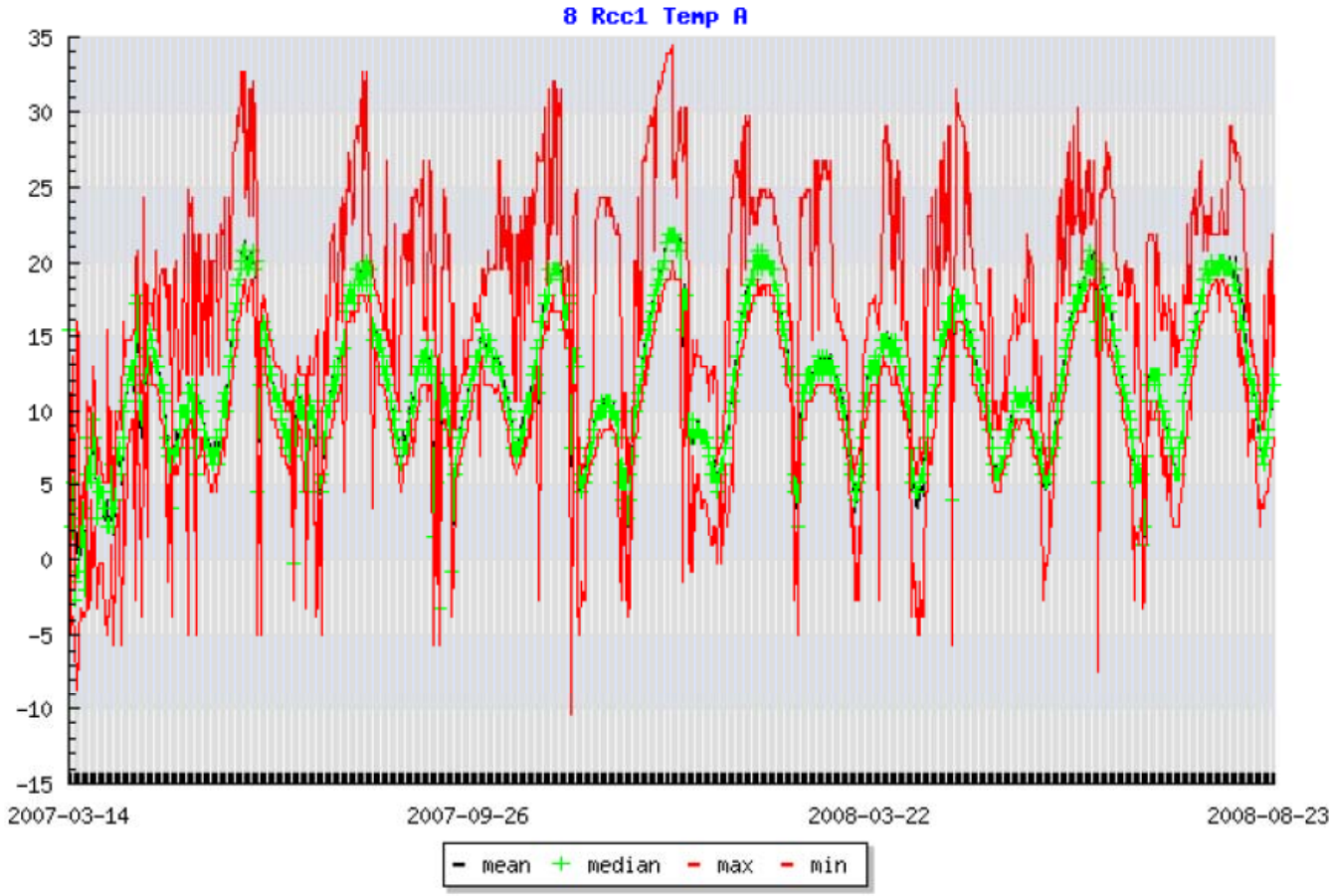




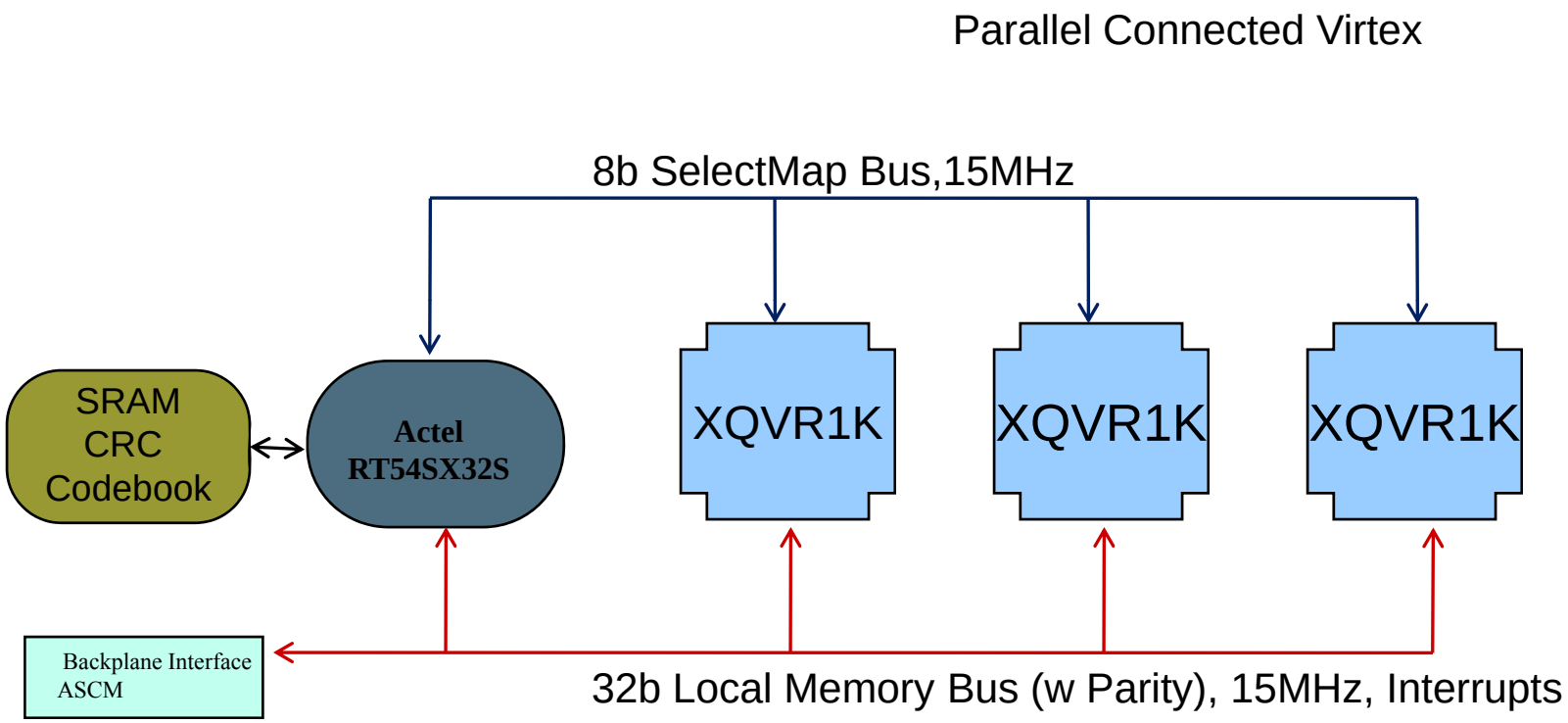
RCC1 Board Level +2.5V Current Consumption



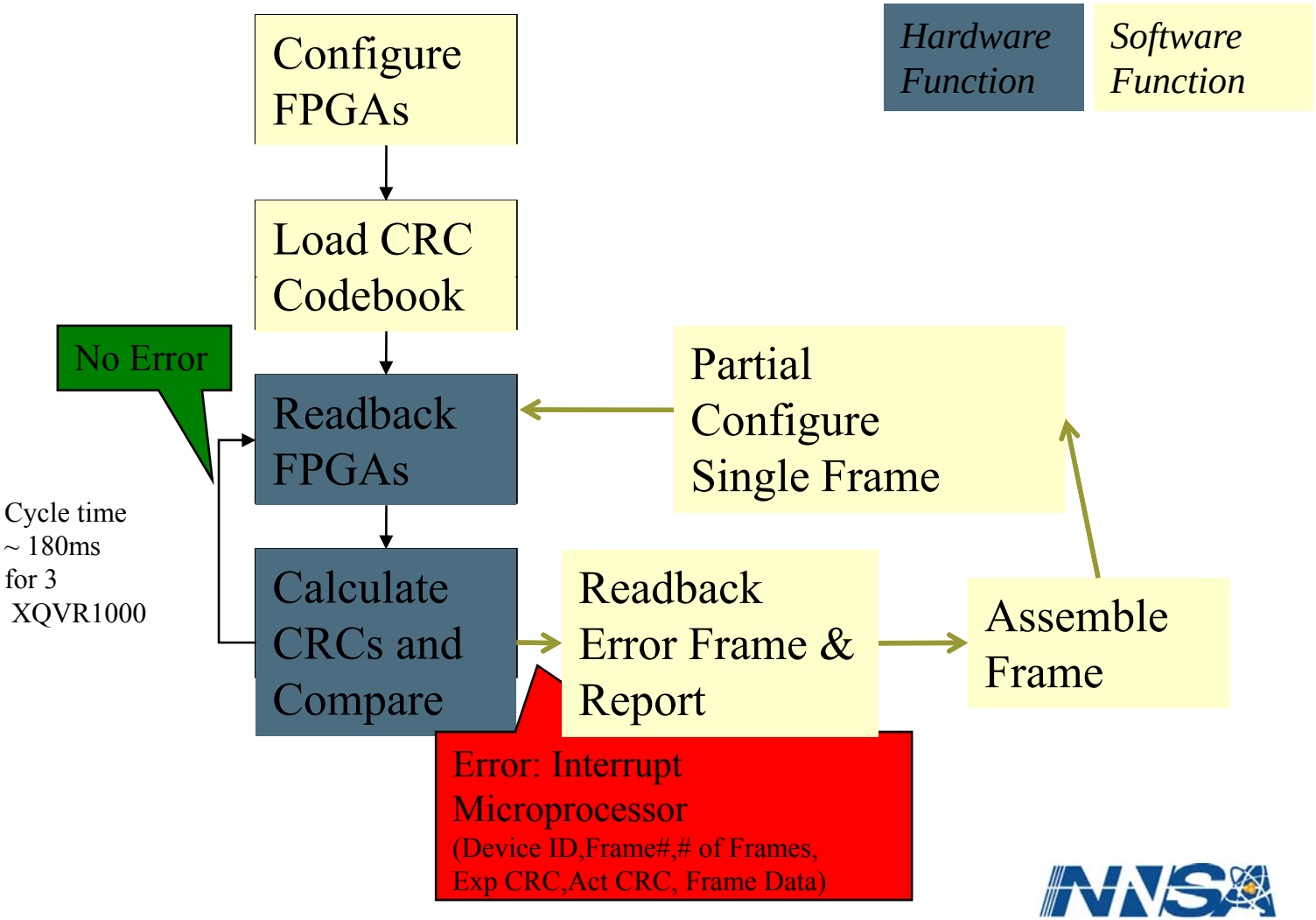
RCC1 FPGA A Die Temperature



Configuration SEU Detection

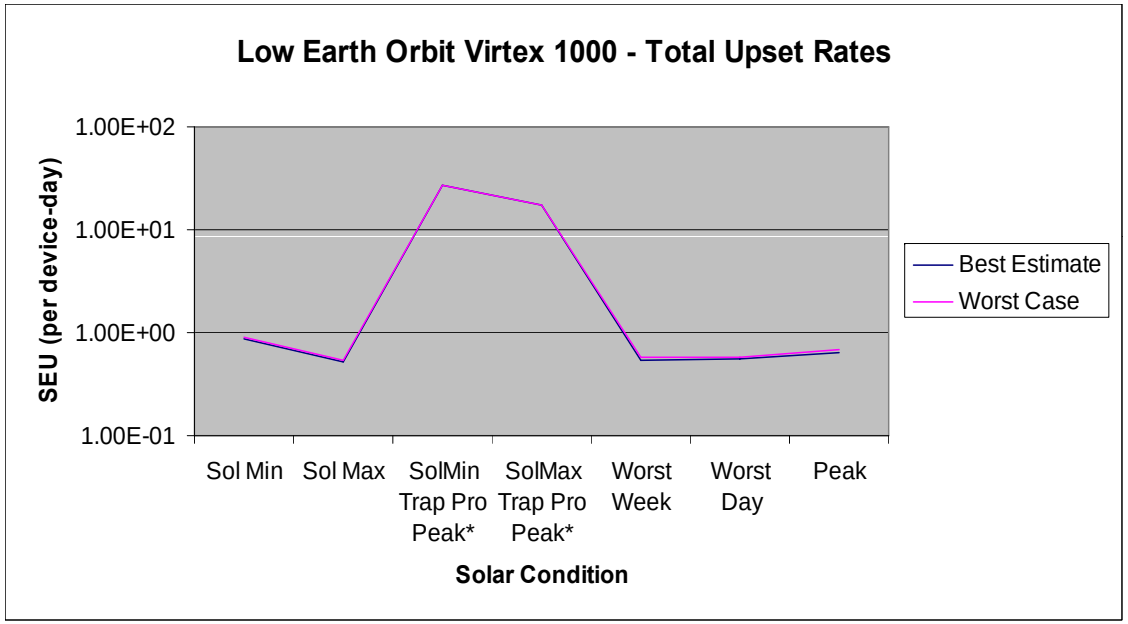


Configuration Bitstream SEU Mitigation Scheme



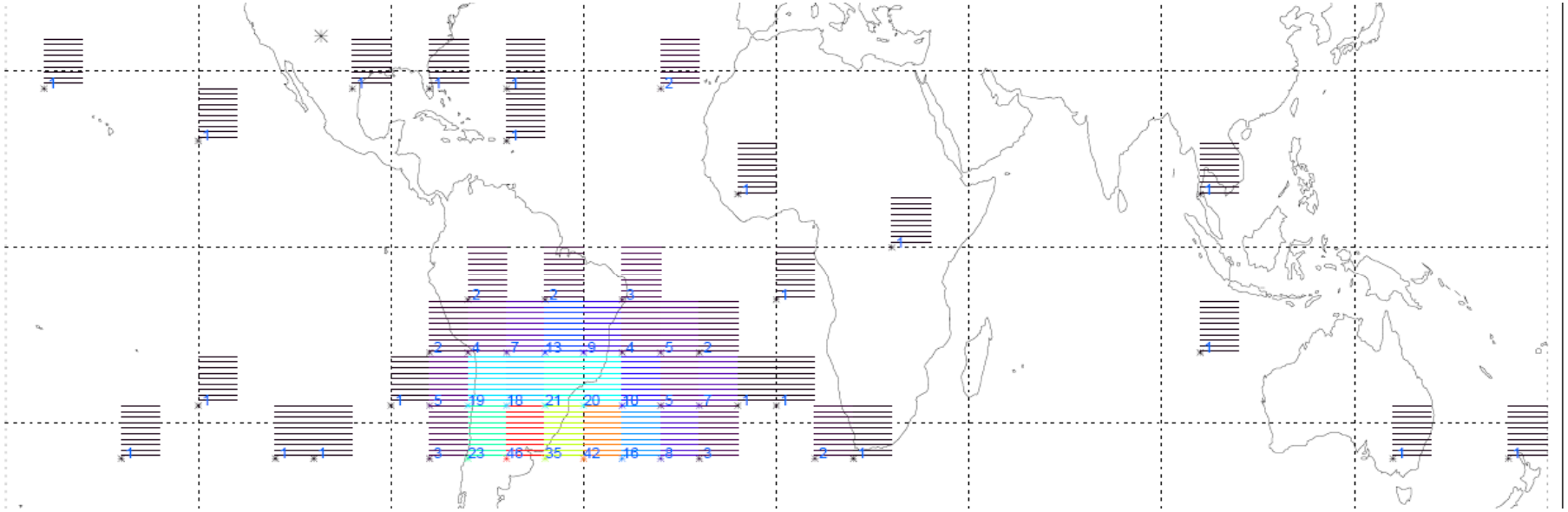
Virtex 1000 LEO SEU Rates Weighted Device Total

Forecast:



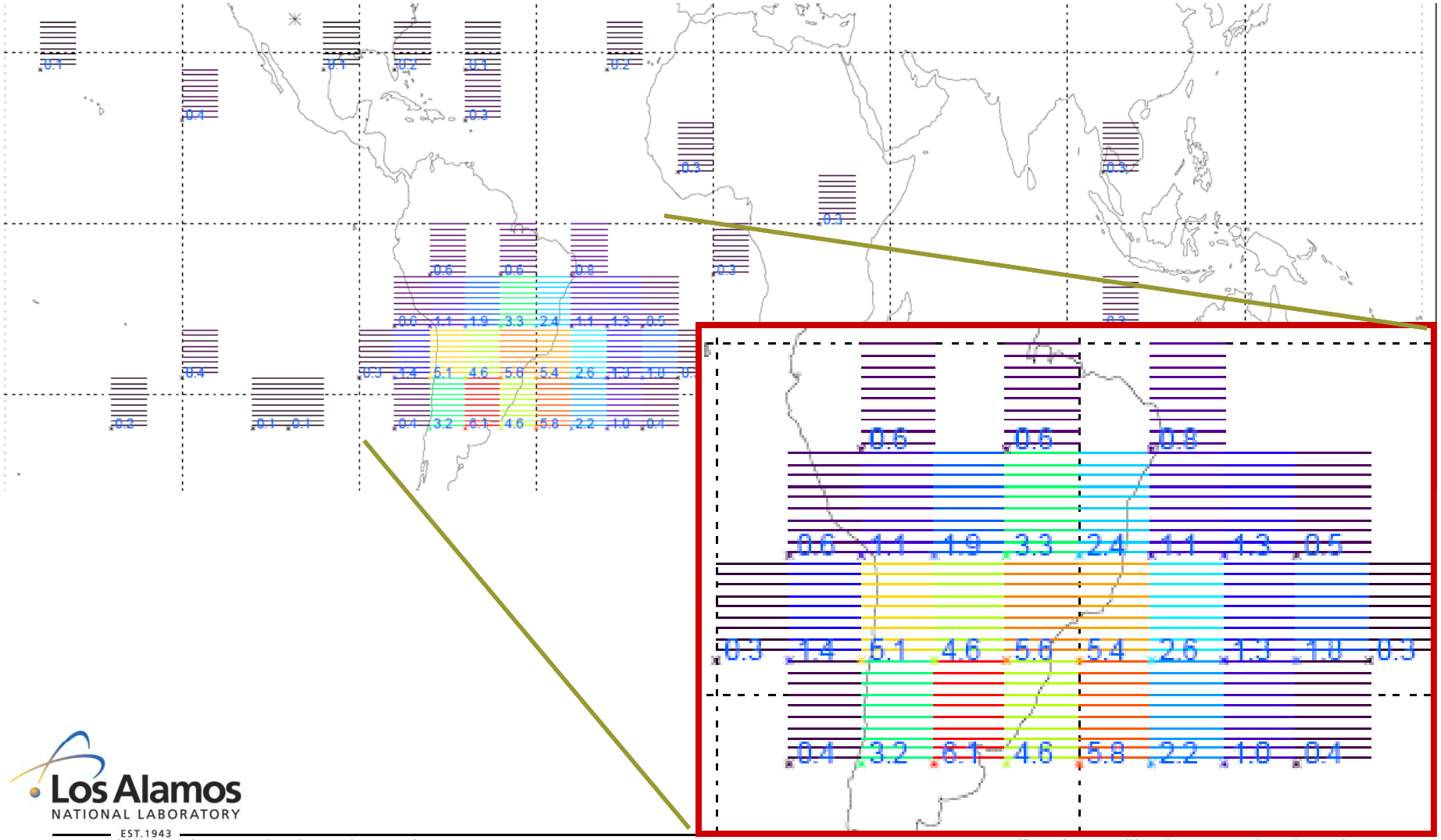
Measured: 365 SEUs / 1380 device days = .26 upsets/device day

Configuration SEUs by Region



- Track the time observing SEUs in each cell
- Record the number, time, type, and location of configuration SEUs

Configuration SEUs / Device Day/ Cell



Future SEU Experiments:
SAVE POWER / THROUGHPUT OVER FULL TMR

- **Survey SEUs in BRAM and SDRAM**
- **Detection**
  - -tool development and validation for smart (full / partial) detection insertion
  - -evaluate detection false alarm rate vs undetected upsets (golden compare)
- **TMR**
  - Full and partial TMR tools need alarm out added
  - Evaluation of alarm signal coverage
- **Domain Specific (software radio)**
  - Evaluate the SNR impact of SEUs on software radio
  - Investigate radio specific schemes for mitigation
    - Eg partition circuit on bit significance or error propagation significance
  - Develop tools for detection and mitigation
- **Detection + Correction**
  - Lightweight model trains on circuit
  - Inputs are available to model if necessary (avoid if possible)
  - SEU results in dual redundancy error detect, model chooses correct output